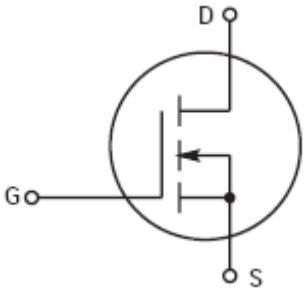
MRF150

RF Power FET
150W, to 150MHz, 50V

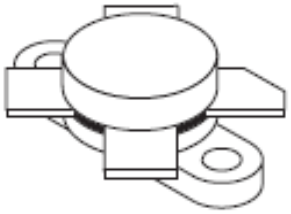
M/A-COM Products
Released - Rev. 9

Designed primarily for linear large-signal output stages up to 150 MHz

- Superior high order IMD
  - IMD(d3) (150W PEP): –32dB (Typ.)
  - IMD(d11) (150W PEP): –60dB (Typ.)
- Specified 50V, 30MHz characteristics
  - Output power = 150 Watts
  - Power gain = 17 dB (Typ.)
  - Efficiency = 45% (Typ.)
- 100% tested for load mismatch at all phase angles



Product Image



CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

NOTE — CAUTION — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	4.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	240	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 30 MHz f = 150 MHz	G_{ps}	— —	17 8.0	— —	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 3.75 A)	η	—	45	—	%
Intermodulation Distortion (1) (V_{DD} = 50 V, P_{out} = 150 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	–32 –60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

CLASS A PERFORMANCE

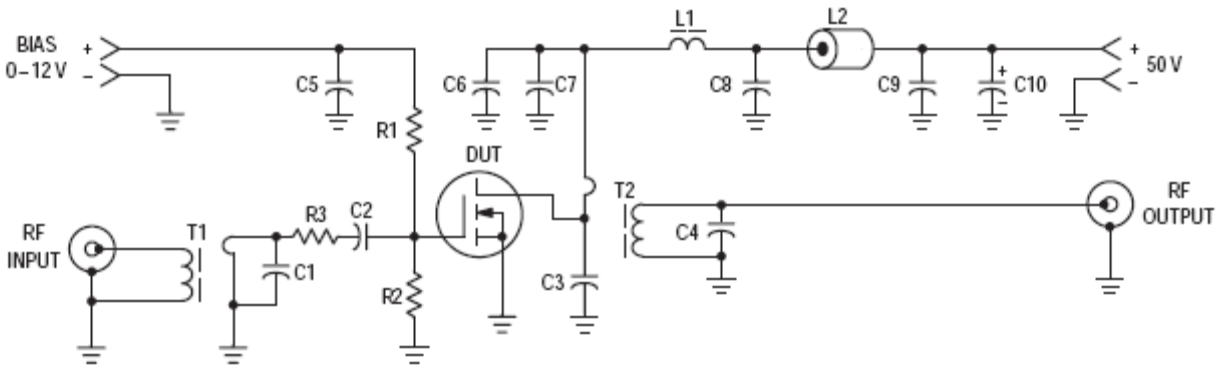
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 3.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 –50 –75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

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C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 µF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 µF/100 V Electrolytic
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 µH
L2 — Ferrite Bead(s), 2.0 µH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer

Figure 1. 30MHz test circuit, 30MHz

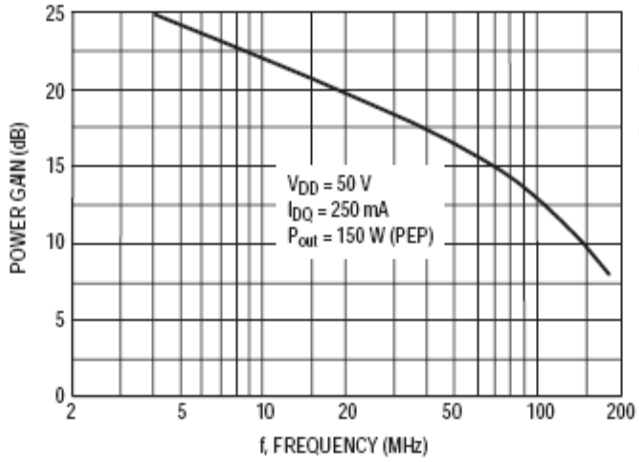


Figure 2. Power Gain versus Frequency

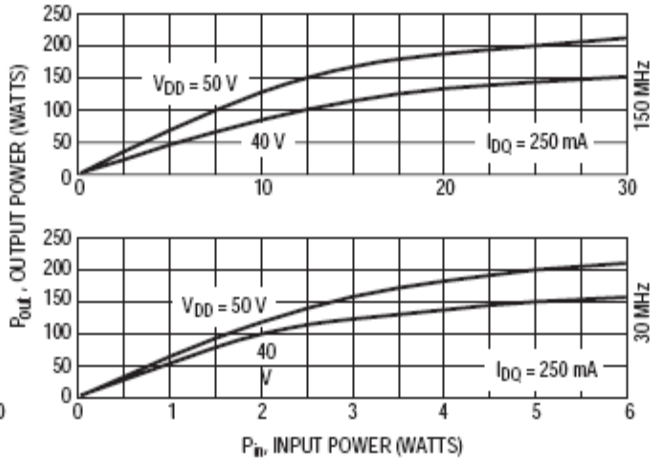


Figure 3. Output Power versus Input Power

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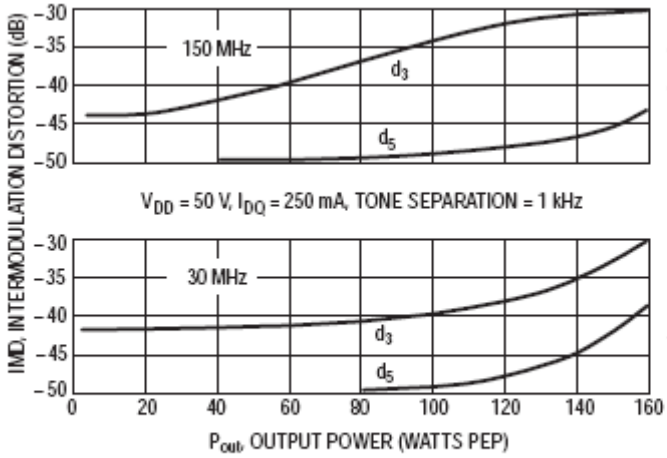


Figure 4. IMD versus P_{out}

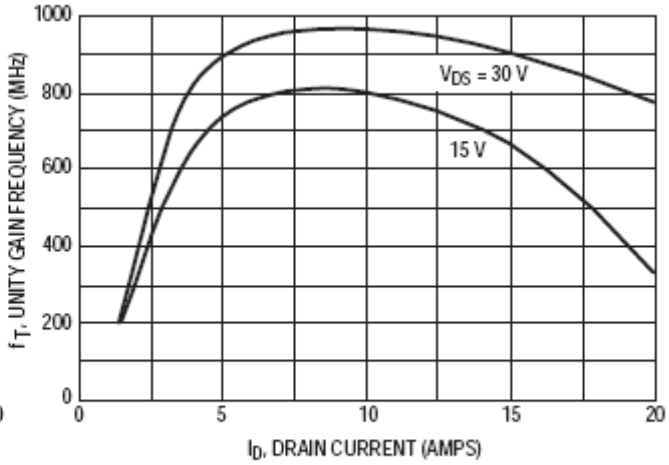


Figure 5. Common Source Unity Gain Frequency versus Drain Current

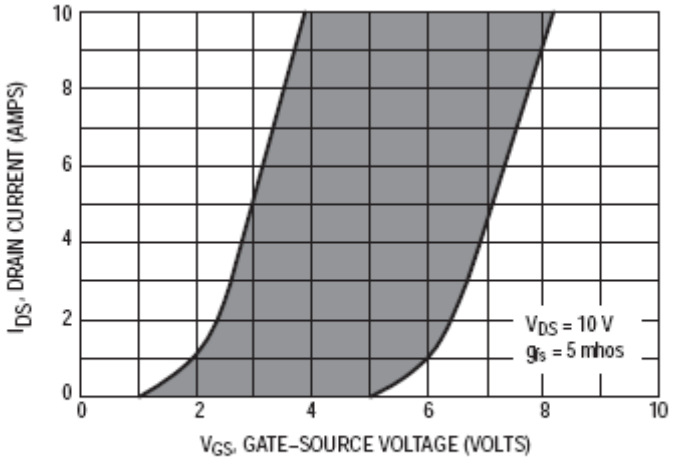


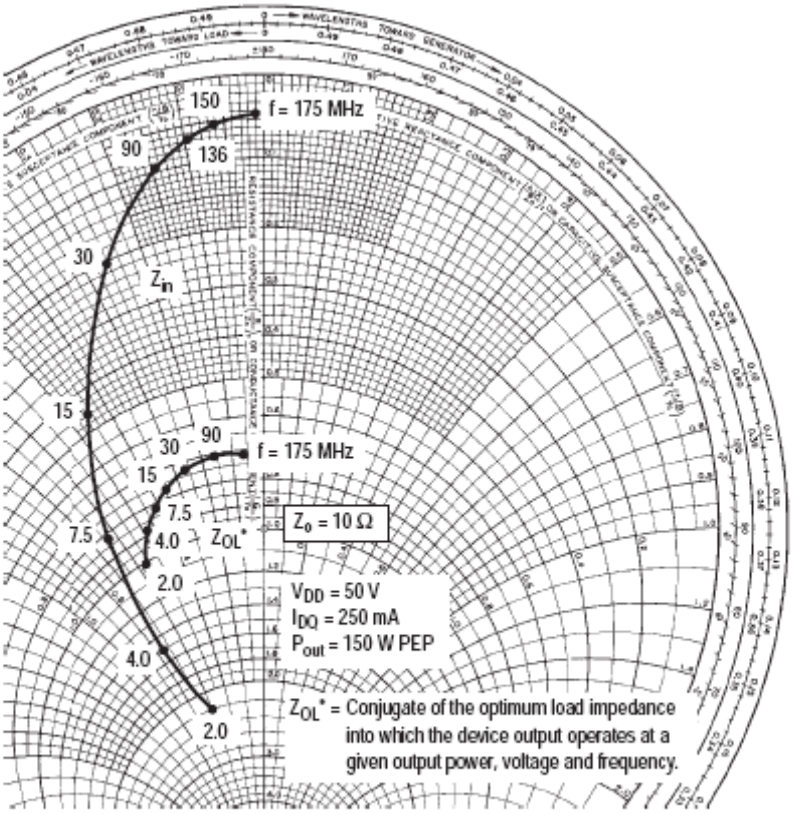
Figure 6. Gate Voltage versus Drain Current

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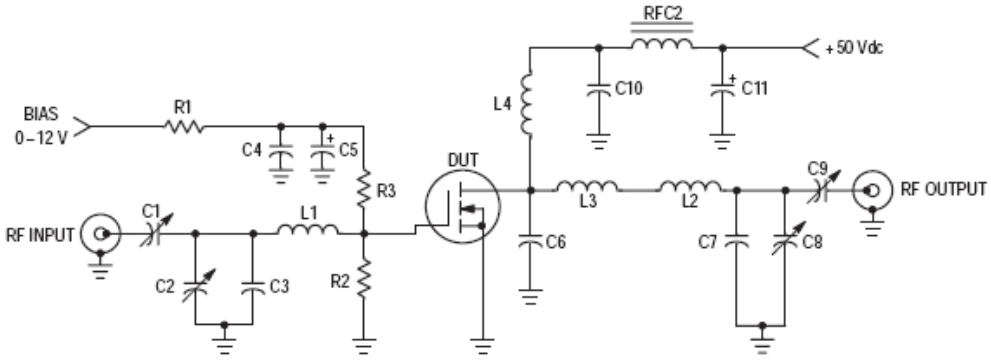
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NOTE: Gate Shunted by 25 Ohms.

Figure 7. Series Equivalent Impedance



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 µF, Ceramic
C5 — 1.0 µF, 15 WV Tantalum
C6 — 25 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 µF, Ceramic
C11 — 15 µF, 60 WV Electrolytic

L1 — 3/4″, 18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 1″, #16 AWG into Hairpin
L4 — 2 Turns #16 AWG, 5/16 ID
RFC1 — 5.6 µH, Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon

Figure 8. 150 MHz Test Circuit (Class AB)

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Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.936	–179	4.13	84	0.011	22	0.844	–176
40	0.936	–179	3.16	79	0.012	23	0.842	–180
50	0.936	–180	2.52	75	0.013	29	0.855	–179
60	0.937	180	2.13	72	0.014	36	0.854	179
70	0.939	179	1.81	68	0.013	42	0.870	179
80	0.940	179	1.53	67	0.013	45	0.868	–179
90	0.941	179	1.34	65	0.014	46	0.855	–178
100	0.942	179	1.21	60	0.016	46	0.874	180
110	0.942	179	1.11	58	0.018	52	0.875	178
120	0.945	178	0.99	56	0.019	61	0.893	180
130	0.946	178	0.88	53	0.019	67	0.902	–179
140	0.947	178	0.83	52	0.019	68	0.919	–179
150	0.949	177	0.74	49	0.020	63	0.910	–179
160	0.949	177	0.71	46	0.024	62	0.889	–180
170	0.952	177	0.65	44	0.026	68	0.878	179
180	0.953	177	0.59	42	0.029	72	0.921	179
190	0.954	176	0.57	41	0.029	75	0.949	178
200	0.956	176	0.52	39	0.028	74	0.929	178
210	0.955	176	0.51	38	0.030	71	0.934	179
220	0.957	175	0.49	35	0.034	70	0.918	177
230	0.960	175	0.43	32	0.039	71	0.977	175
240	0.959	175	0.42	32	0.040	74	0.941	175
250	0.961	175	0.39	32	0.040	77	0.944	176
260	0.961	175	0.36	31	0.040	76	0.948	177
270	0.960	174	0.35	29	0.043	74	0.947	175
280	0.963	174	0.34	29	0.046	73	0.929	174
290	0.963	174	0.32	25	0.048	74	0.918	172
300	0.965	173	0.32	28	0.051	78	0.925	174
310	0.966	173	0.29	27	0.052	79	0.953	174
320	0.963	173	0.28	26	0.054	76	0.954	172
330	0.965	172	0.26	22	0.057	74	0.914	171
340	0.966	172	0.26	27	0.058	72	0.925	171
350	0.965	172	0.26	25	0.062	75	0.934	171
360	0.968	171	0.25	25	0.065	74	0.979	171
370	0.967	171	0.23	24	0.064	73	0.993	168
380	0.967	171	0.24	22	0.068	74	0.952	172
390	0.969	170	0.22	26	0.069	74	0.942	170
400	0.968	170	0.21	23	0.072	76	0.936	172
410	0.968	170	0.21	24	0.076	73	0.984	168
420	0.970	169	0.20	25	0.078	71	0.977	167
430	0.969	169	0.18	25	0.082	72	0.959	168
440	0.970	169	0.19	25	0.082	73	0.953	169

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f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
450	0.971	168	0.19	24	0.085	75	0.960	168
460	0.972	168	0.17	26	0.086	70	0.960	164
470	0.972	168	0.17	23	0.087	70	0.952	165
480	0.969	167	0.18	26	0.093	70	0.977	166
490	0.969	167	0.18	25	0.099	71	0.966	166
500	0.969	166	0.17	26	0.101	71	0.972	164

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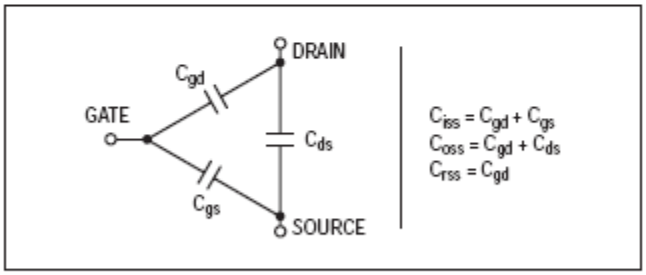
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

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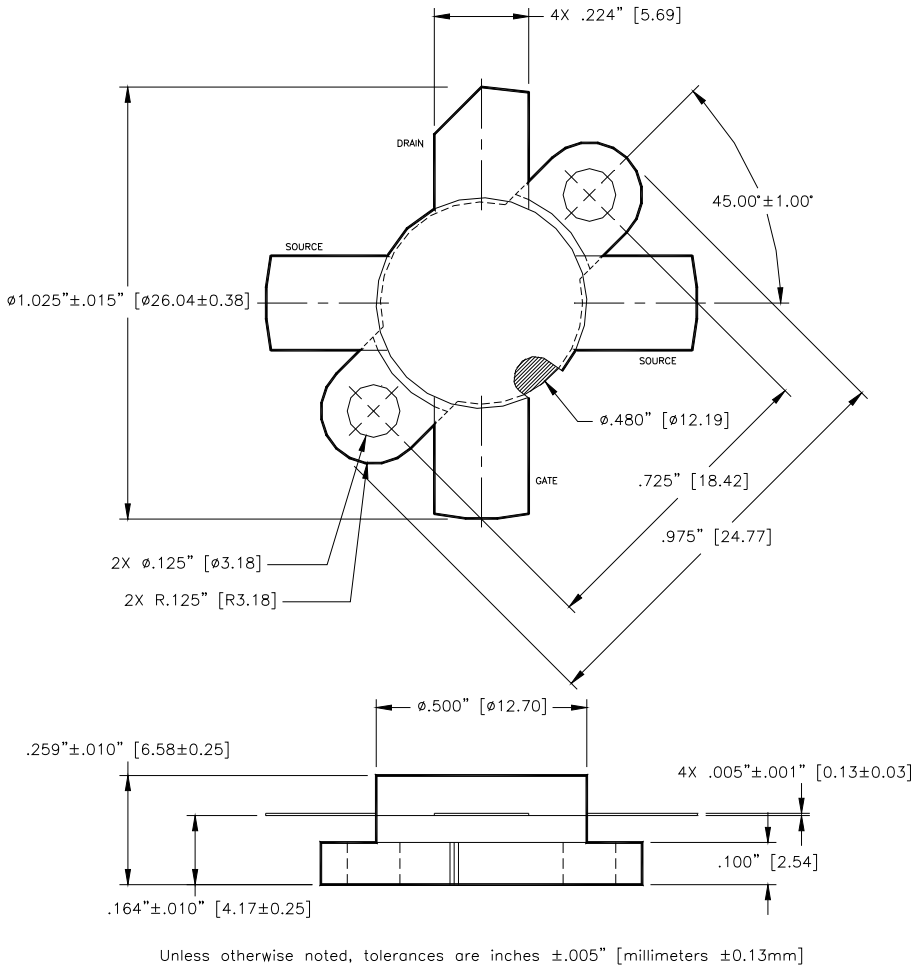
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EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}

$$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C} \qquad r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$$



Unless otherwise noted, tolerances are inches ±.005" [millimeters ±0.13mm]

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