WIZ550io

WIZ550io

Overview

WIZ550io is an auto configurable Ethernet controller that includes a W5500 (TCP/IP hardwired chip and PHY embedded), a transformer and RJ45.

It has a unique real MAC address and configures the network setting automatically. When powered on, WIZ550io initializes itself … with embedded real MAC and sets the default IP address (192.168.1.2) and it can be pinged. Therefore, users are not required to write MAC and network information like IP address, Subnet mask and Gateway address. The WIZ550io is an ideal product for users who want to develop their Internet enabling systems rapidly.

For more information on the W5500 chip inside the WIZ550io module please also refer to the chip's datasheet:

Datasheet

- W5500 Datasheet v1.0.2 - English
- W5500 Datasheet v1.0.2 - Korean

Datasheet History

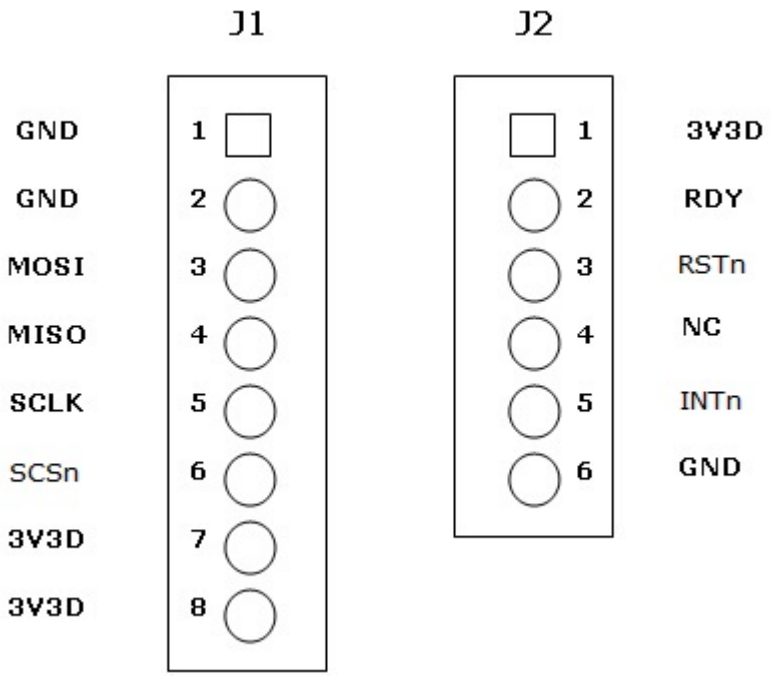
Version	Date	Description
1.0.0	2013-08-01	Initial Release

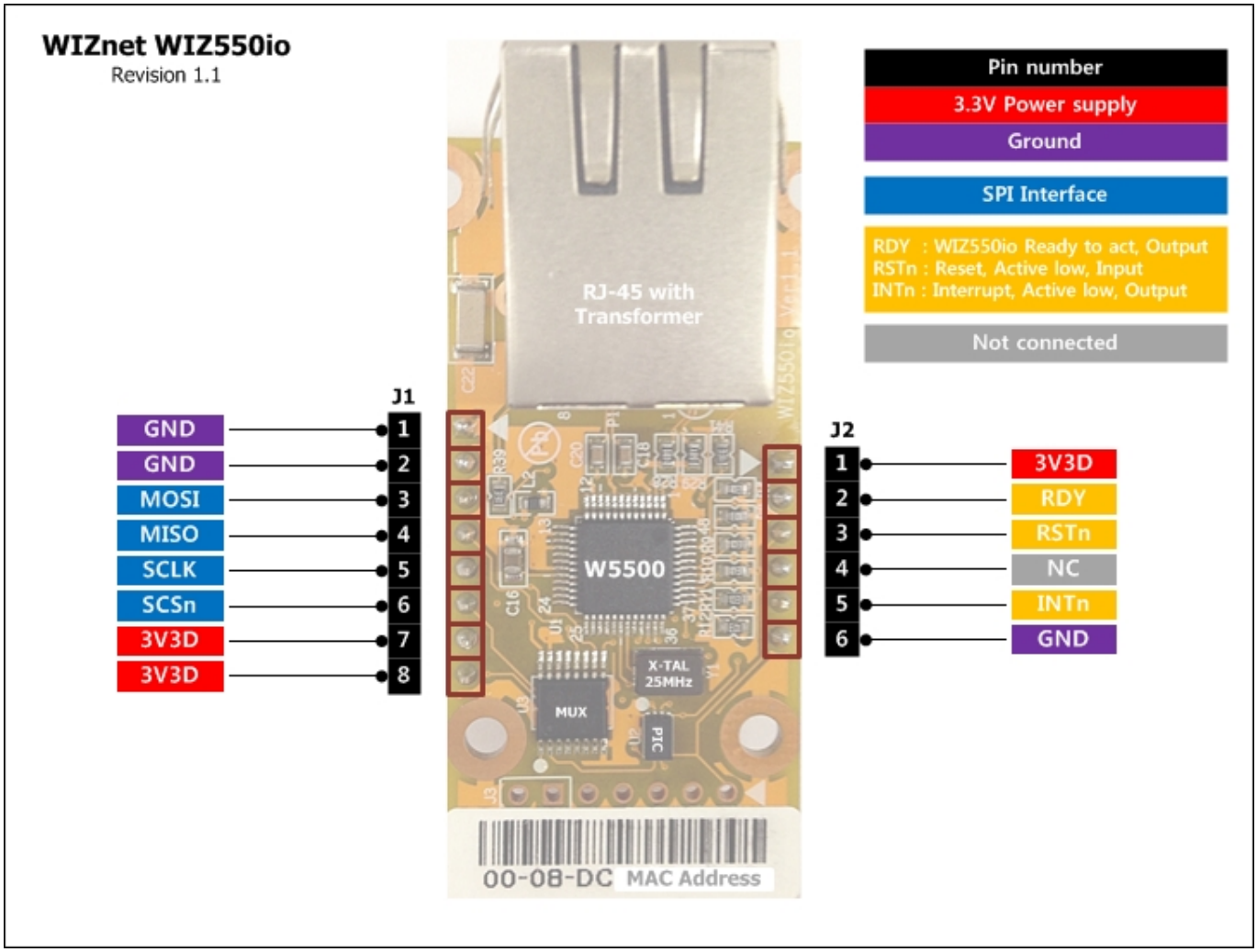
1.0.1	2013-09-13	Corrected duplicated statements and typing errors (P.14, 23, 24, 28, 39, 51) Corrected descriptions (P.35)
1.0.2	2013-11-14	Changed *"descriptions of pin at 1.1 Pin Descriptions"* (P.10) starting "It must be tied to GND to NC (PIN38..42)" / 2. corrected typing error: starting "0x02 to 0x42 value of SOCK_MACRAW at 4.2 Socket Registers(P.50)"

2013/08/30 10:01 · bongbong
2013/08/28 09:00 · jameskim

Hardware Pins of WIZ550io

Pin Map





Pin Description

Pin No.		I/O	Pin Name	Description
J1	1	P	GND	Ground
	2	P	GND	Ground
	3	I	MOSI	**SPI Master Out Slave In** This pin is used for SPI MOSI signal pin
	4	O	MISO	**SPI Master In Slave Out** This pin is used for SPI MISO signal pin
	5	I	SCLK	**SPI Clock** This pin is used for SPI Clock Signal pin
	6	I	SCSn	**SPI Slave Select** This pin is used for SPI Slave Select Signal Pin when using SPI interface
	7	P	3V3D	**Power**: 3.3V Power Supply
	8	P	3V3D	**Power**: 3.3V Power Supply

Pin No.	I/O	Pin Name	Description

J2	1	P	3V3D	**Power**: 3.3V Power Supply
	2	O	RDY	**READY** This pin is asserted to low after power on. When RSTn is activated, WIZ550io does auto configuration with embedded MAC and default IP address. After configuration gets completed, WIZ550io raises this pin to HIGH in order to inform about the completion of WIZ550io's configuration. Host processor can only control WIZ55oio when RDY pin is HIGH.
	3	I	RSTn	**Reset**: Low activity This pin is to initialize WIZ550io. Hold at least 500us after asserted to LOW and wait for at least 150ms after it is changed to HIGH until WIY550io configured itself.
	4	I	NC	**Not Connected**
	5	O	INTn	**Interrupt**: Low activity This pin indicates that W5500 inside WIZ550io requires MCU's due to events like socket connection, disconnection, data receiving timeout and WOL (Wake on Lan). The interrupt is cleared by writing IR register or Sn_IR. All interrupts are maskable.
	6	P	GND	**Ground**

Caution)
Some users may want to reinitialize W5500 inside WIZ550io with SW reset, not handling RSTn pin. It will make WIZ550io hang up due to clearance of all information in the registers of W5500. A tiny MCU inside WIZ550io initializes W5500 with embedded MAC address and a default IP address and Initialization is triggered by RSTn.

In case of SW reset, all registers in W5500 will be cleared and WIZ550io will not initialize itself. All information inside WIZ550io will be lost and WIZ550io will hang up instead.

Therefore, we recommend HW reset instead of SW reset. Nevertheless, if users want to use SW reset, we recommend to save MAC address and network information including IP address, Subnet mask and Gateway address before SW reset, and writing those information to WIZ550io after SW reset.

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SPI Operations

There is a W5500 inside WIZ550io. Therefore SPI operation of WIZ550io follows one of W5500. For more information about SPI operation of WIZ550io, please refer to W5500 Datasheet.

Datasheet

- W5500 Datasheet v1.0.2 - English
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Datasheet History

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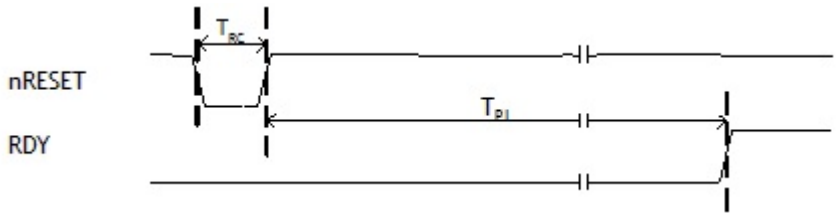
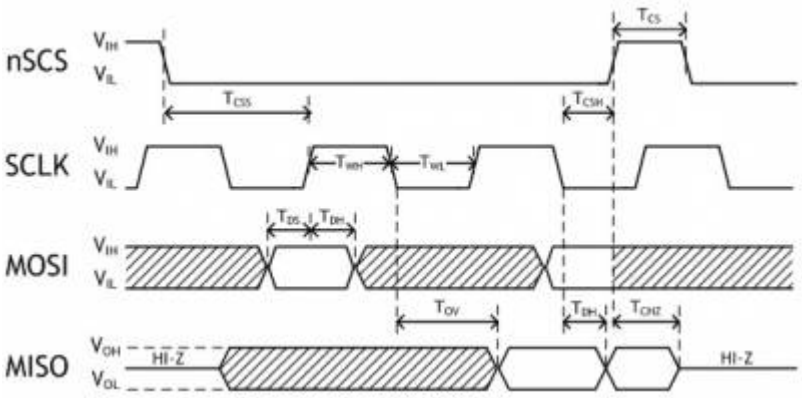
Timing Diagram

Reset Timing



Symbol	Description	Min	Max
TRC	Reset Cycle Time	500us	-
TPL	Internal Auto Configuration Time	-	50ms

SPI Timing



Symbol	Description	Min	Max	Units
Fsck	SCLK Clock Frequency	-	80	MHz

TWH	SCLK High duration	6	-	ns
TWL	SCLK Low duration	6	-	ns
TCS	nSCS High duration	5	-	ns

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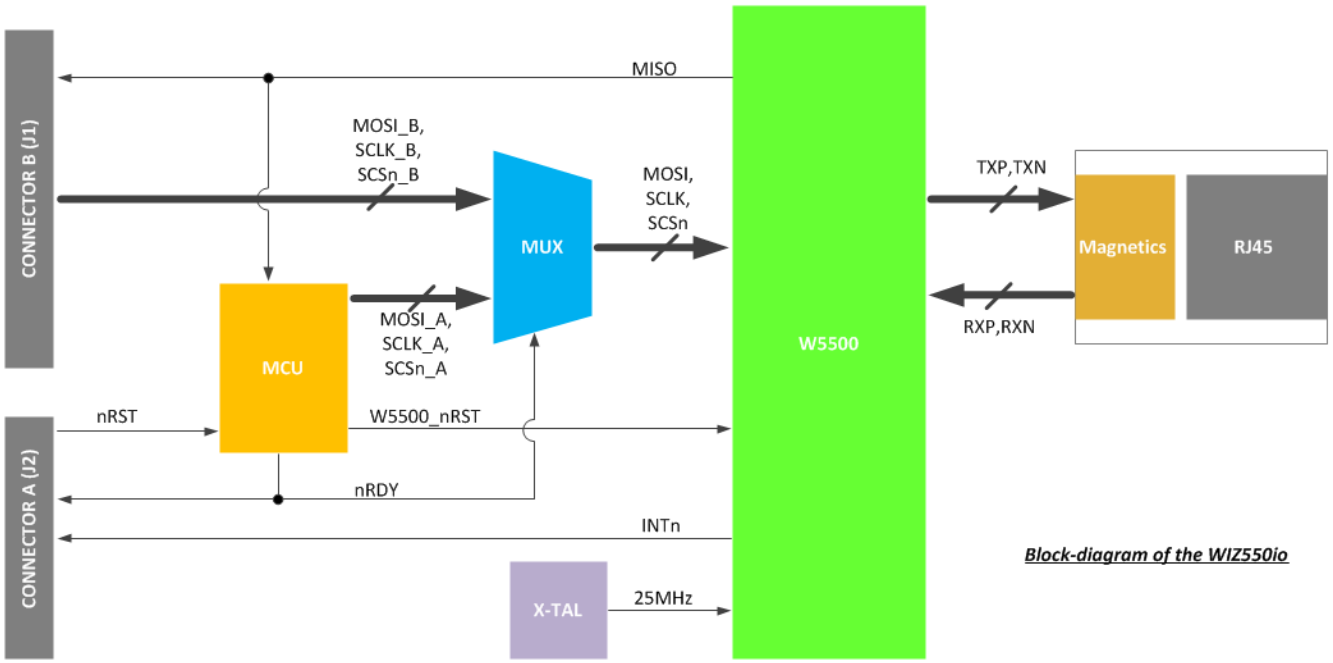
Block Diagram



Schematic

- Revision 1.1 WIZ550io Rev1.1 Schematic

BOM

- V1.1

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Dimension

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WIZ550io Ver1.0
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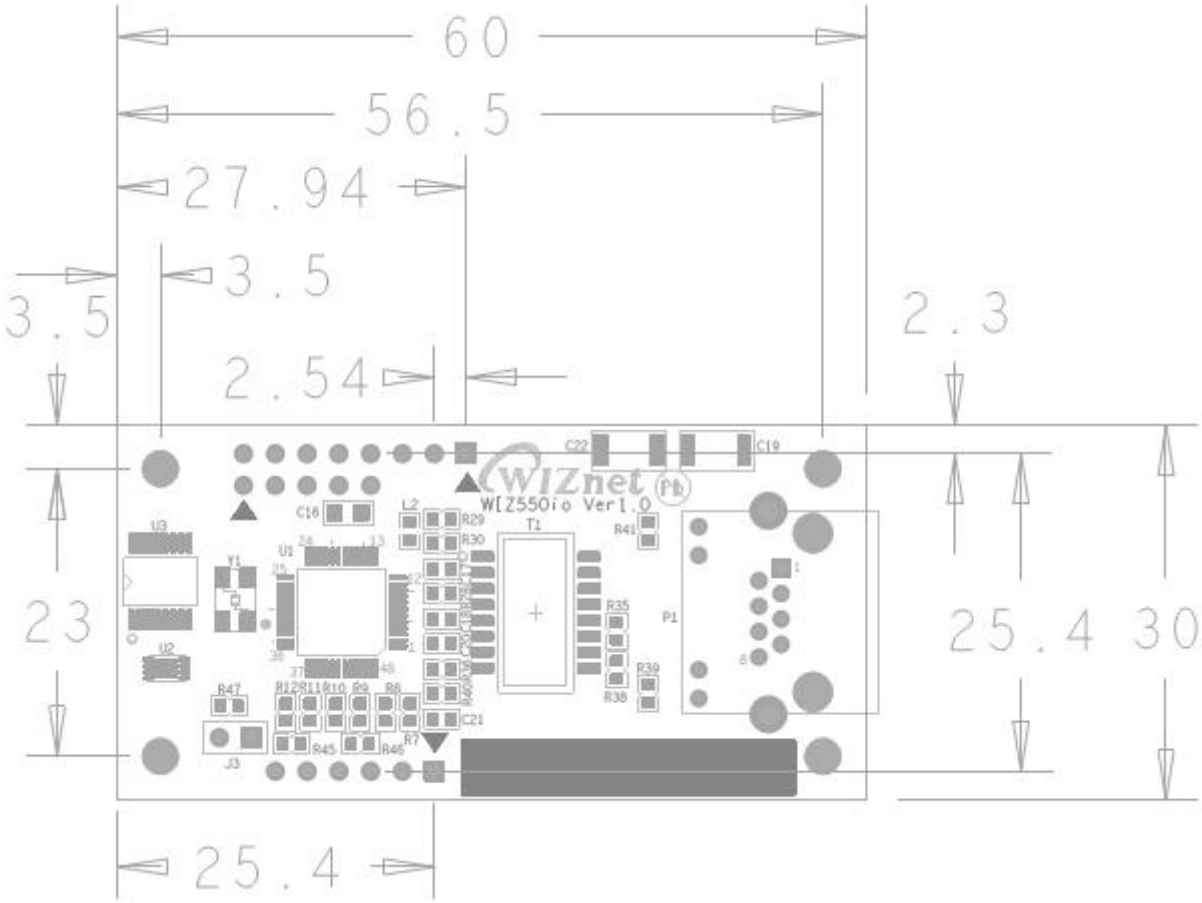
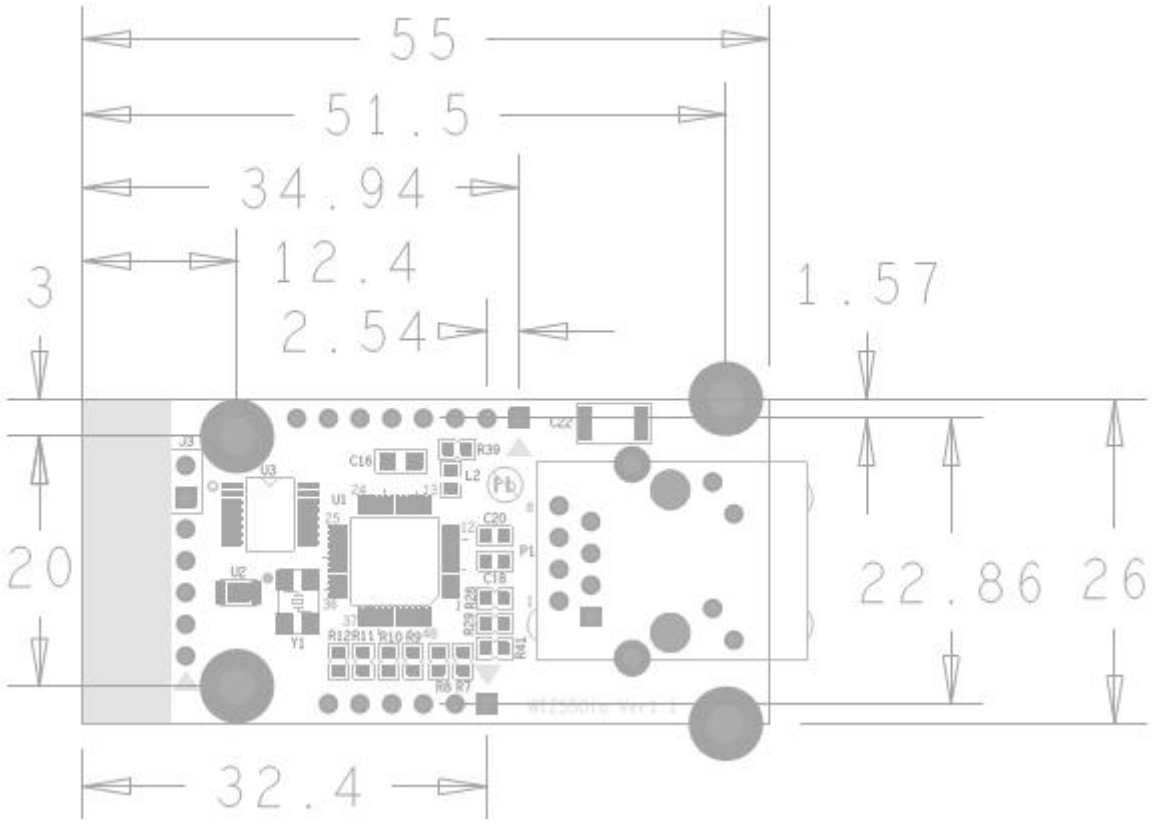


WIZ550io Ver1.1



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Related Products

- ioShield-A
- ioShield-K
- ioShield-L

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