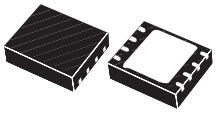
# ST1S10

## 3 A, 900 kHz, monolithic synchronous step-down regulator IC

**Datasheet - production data**



**DFN8 (4 x 4 mm)**

**PowerSO-8**

## Features

- Step-down current mode PWM regulator
- Output voltage adjustable from 0.8 V
- Input voltage from 2.5 V up to 18 V
- 2% DC output voltage tolerance
- Synchronous rectification
- Inhibit function
- Synchronizable switching frequency from 400 kHz up to 1.2 MHz
- Internal soft start
- Dynamic short-circuit protection
- Typical efficiency: 90%
- 3 A output current capability
- Standby supply current: max. 6 µA over temperature range
- Operative junction temp.: from -40 °C to 125 °C

## Applications

- Consumer
  - STB, DVD, DVD recorders, TV, VCR, car audio, LCD monitors
- Networking
  - XDSL, modems, DC-DC modules
- Computer
  - Optical storage, HD drivers, printers, audio/graphic cards
- Industrial and security
  - Battery chargers, DC-DC converters, PLD, PLA, FPGA, LED drivers

## Description

The ST1S10 is a high efficiency step-down PWM current mode switching regulator capable of providing up to 3 A of output current. The device operates with an input supply range from 2.5 V to 18 V and provides an adjustable output voltage from 0.8 V ($V_{FB}$) to 0.85 * $V_{IN\_SW}$ [$V_{OUT} = V_{FB} * (1 + R1/R2)$]. It operates either at a 900 kHz fixed frequency or can be synchronized to an external clock (from 400 kHz to 1.2 MHz). The high switching frequency allows the use of tiny SMD external components, while the integrated synchronous rectifier eliminates the need for a Schottky diode. The ST1S10 provides excellent transient response, and is fully protected against thermal overheating, switching overcurrent and output short-circuit.

The ST1S10 is the ideal choice for point of load regulators or LDO pre-regulation.

**Table 1. Device summary**

| Part number | Order codes | |
|---|---|---|
| | DFN8 (4 x 4 mm) | PowerSO-8 |
| ST1S10 | ST1S10PUR | ST1S10PHR |

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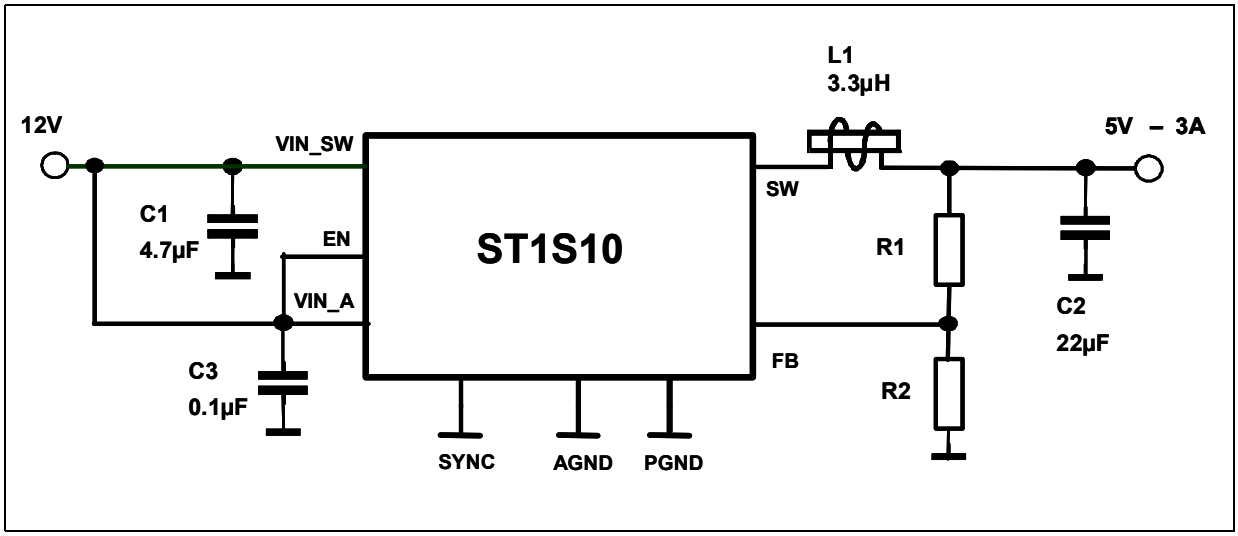
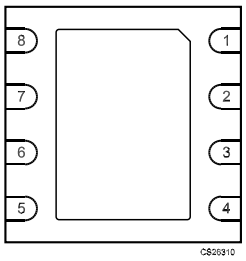
# 1 Application circuit

Figure 1. Typical application circuit

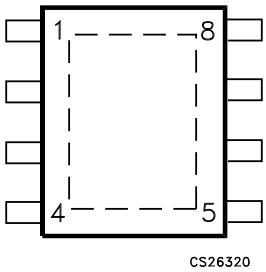


# 2 Pin configuration

**Figure 2. Pin connections (top view for PowerSO-8, bottom view for DFN8)**




DFN8 (4x4)




PowerSO-8

**Table 2. Pin description**

| Pin no. | Symbol | Name and function |
|---|---|---|
| 1 | $V_{IN\_A}$ | Analog input supply voltage to be tied to $V_{IN}$ supply source |
| 2 | INH (EN) | Inhibit pin active low. Connect to $V_{IN\_A}$ if not used |
| 3 | $V_{FB}$ | Feedback voltage for connection to external voltage divider to set the $V_{OUT}$ from 0.8V up to 0.85*$V_{IN\_SW}$. (see *Section 5.5: Output voltage selection on page 13*) |
| 4 | AGND | Analog ground |
| 5 | SYNC | Synchronization and frequency select. Connect SYNC to GND for 900 kHz operation, or to an external clock from 400 kHz to 1.2 MHz. (see *Section 5.8.1: Sync operation on page 14*) |
| 6 | $V_{IN\_SW}$ | Power input supply voltage to be tied to $V_{IN}$ power supply source |
| 7 | SW | Switching node to be connected to the inductor |
| 8 | PGND | Power ground |
| epad | epad | Exposed pad to be connected to ground |

# 3 Maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{IN\_SW}$ | Positive power supply voltage | -0.3 to 20 | V |
| $V_{IN\_A}$ | Positive supply voltage | -0.3 to 20 | V |
| $V_{INH}$ | Inhibit voltage | -0.3 to $V_{IN\_A}$ | V |
| $V_{SW}$ | Output switch voltage | -0.3 to 20 | V |
| $V_{FB}$ | Feedback voltage | -0.3 to 2.5 | V |
| $I_{FB}$ | FB current | -1 to +1 | mA |
| Sync | Synchronization | -0.3 to 6 | V |
| $T_{STG}$ | Storage temperature range | -40 to 150 | °C |
| $T_{OP}$ | Operating junction temperature range | -40 to 125 | °C |

*Note: Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 4. Thermal data**

| Symbol | Parameter | PowerSO-8 | DFN8 | Unit |
|---|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction ambient | 40 | 40 | °C/W |
| $R_{thJC}$ | Thermal resistance junction case | 12 | 4 | °C/W |

**Table 5. ESD protection**

| Symbol | Test condition | Value | Unit |
|---|---|---|---|
| ESD | HBM | 2 | kV |
| | CDM | 500 | V |
| | MM | 200 | V |

# 4 Electrical characteristics

$V_{IN} = V_{IN\_SW} = V_{IN\_A} = V_{INH}$ = 12 V, $V_{SYNC}$ = GND, $V_{OUT}$ = 5 V, $I_{OUT}$ = 10 mA, $C_{IN}$ = 4.7 µF +0.1 µF, $C_{OUT}$ = 22 µF, L1 = 3.3 µH, $T_J$ = -40 to 125 °C (unless otherwise specified, refer to the typical application circuit. Typical values assume $T_J$ = 25 °C).

**Table 6. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback voltage | $T_J$ = 25 °C | 784 | 800 | 816 | mV |
| | | $T_J$ = -25 °C to 125 °C | 776 | 800 | 824 | mV |
| $I_{FB}$ | $V_{FB}$ pin bias current | | | | 600 | nA |
| $I_Q$ | Quiescent current | $V_{INH}$ > 1.2 V, not switching | | 1.5 | 2.5 | mA |
| | | $V_{INH}$ < 0.4 V | | 2 | 6 | µA |
| $I_{OUT}$ | Output current(1) | $V_{IN}$ = 2.5 V to 18 V $V_{OUT}$ = 0.8 V to 13.6 V (2) | 3.0 | | | A |
| $V_{INH}$ | Inhibit threshold | Device ON | 1.2 | | | V |
| | | Device OFF | | | 0.4 | V |
| $I_{INH}$ | Inhibit pin current | | | 2 | | µA |
| $\%V_{OUT}/\Delta V_{IN}$ | Reference line regulation | 2.5 V < $V_{IN}$ < 18 V | | 0.4 | | $\%V_{OUT}/\Delta V_{IN}$ |
| $\%V_{OUT}/\Delta I_{OUT}$ | Reference load regulation | 10 mA < $I_{OUT}$ < 3 A | | 0.5 | | $\%V_{OUT}/\Delta I_{OUT}$ |
| PWM fs | PWM switching frequency | $V_{FB}$ = 0.7 V, Sync = GND $T_J$ = 25 °C | 0.7 | 0.9 | 1.1 | MHz |
| $D_{MAX}$ | Maximum duty cycle(2) | | 85 | 90 | | % |
| $R_{DSon}$-N | NMOS switch on resistance | $I_{SW}$ = 750 mA | | 0.10 | | Ω |
| $R_{DSon}$-P | PMOS switch on resistance | $I_{SW}$ = 750 mA | | 0.12 | | Ω |
| $I_{SWL}$ | Switch current limitation | | | 5.0 | | A |
| ν | Efficiency | $I_{OUT}$ = 100 mA to 300 mA | | 85 | | % |
| | | $I_{OUT}$ = 300 mA to 3 A | | 90 | | % |
| $T_{SHDN}$ | Thermal shutdown | | | 150 | | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | 15 | | °C |
| $V_{OUT}/\Delta I_{OUT}$ | Output transient response | 100 mA < $I_{OUT}$ < 1 A, $t_R = t_F \geq$ 500 ns | | ±5 | | $\%V_O$ |
| $V_{OUT}/\Delta I_{OUT}$ @$I_O$=short | Short-circuit removal response (overshot) | 10 mA < $I_{OUT}$ < short | | ±10 | | $\%V_O$ |
| $F_{SYNC}$ | SYNC frequency capture range | $V_{IN}$ = 2.5 V to 18 V, $V_{SYNC}$ = 0 to 5 V | 0.4 | | 1.2 | MHz |
| $SYNC_{WD}$ | SYNC pulse width | $V_{IN}$ = 2.5 V to 18 V | 250 | | | ns |
| $V_{IL\_SYNC}$ | SYNC input threshold low | $V_{IN}$ = 2.5 V to 18 V | | | 0.4 | V |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH\_SYNC}$ | SYNC input threshold high | $V_{IN}$ = 2.5 V to 18 V | 1.6 | | | V |
| $I_{IL}$, $I_{IH}$ | SYNC input current | $V_{IN}$ = 2.5 V to 18 V, $V_{SYNC}$ = 0 or 5 V | -10 | | +10 | µA |
| UVLO | Under voltage lock-out threshold | $V_{IN}$ rising | | 2.3 | | V |
| | | Hysteresis | | 200 | | mV |

1. Guaranteed by design, but not tested in production.
2. See *Section 5.5: Output voltage selection* for maximum duty cycle conditions.

# 5 Application information

## 5.1 Description

The ST1S10 is a high efficiency synchronous step-down DC-DC converter with inhibit function. It provides up to 3 A over an input voltage range of 2.5 V to 18 V, and the output voltage can be adjusted from 0.8 V up to 85% of the input voltage level. The synchronous rectification removes the need for an external Schottky diode and allows higher efficiency even at very low output voltages.

A high internal switching frequency (0.9 MHz) allows the use of tiny surface-mount components, as well as a resistor divider to set the output voltage value. In typical application conditions, only an inductor and 3 capacitors are required for proper operation.

The device can operate in PWM mode with a fixed frequency or synchronized to an external frequency through the SYNC pin. The current mode PWM architecture and stable operation with low ESR SMD ceramic capacitors results in low, predictable output ripple. No external compensation is needed.

To maximize power conversion efficiency, the ST1S10 works in pulse skipping mode at light load conditions and automatically switches to PWM mode when the output current increases.

The ST1S10 is equipped with thermal shutdown protection activated at 150 °C (typ.).

Cycle-by-cycle short-circuit protection provides protection against shorted outputs for the application and the regulator. An internal soft start for start-up current limiting and power ON delay of 275 µs (typ.) helps to reduce inrush current during start-up.

## 5.2 External components selection

### Input capacitor

The ST1S10 features two $V_{IN}$ pins: $V_{IN\_SW}$ for the power supply input voltage where the switching peak current is drawn, and $V_{IN\_A}$ to supply the ST1S10 internal circuitry and drivers.

The $V_{IN\_SW}$ input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. A high power supply source impedance requires larger input capacitance.

For the $V_{IN\_SW}$ input capacitor the RMS current rating is a critical parameter that must be higher than the RMS input current. The maximum RMS input current can be calculated using the following equation:

**Equation 1**

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

where $\eta$ is the expected system efficiency, $D$ is the duty cycle and $I_O$ is the output DC current. The duty cycle can be derived using *Equation 2*.

**Equation 2**

$$D = (V_{OUT} + V_F) / (V_{IN}-V_{SW})$$

where $V_F$ is the voltage drop across the internal NMOS, and $V_{SW}$ represents the voltage drop across the internal PDMOS. The minimum duty cycle (at $V_{IN\_max}$) and the maximum duty cycle (at $V_{IN\_min}$) should be considered in order to determine the max $I_{RMS}$ flowing through the input capacitor.

A minimum value of 4.7 µF for the $V_{IN\_SW}$ and a 0.1 µF ceramic capacitor for the $V_{IN\_A}$ are suitable in most application conditions. A 10 µF or higher ceramic capacitor for the $V_{IN\_SW}$ and a 1 µF or higher for the $V_{IN\_A}$ are recommended in cases of higher power supply source impedance or where long wires are needed between the power supply source and the $V_{IN}$ pins. The above higher input capacitor values are also recommended in cases where an output capacitive load is present (47 µF < $C_{LOAD}$ < 100 µF), which could impact the switching peak current drawn from the input capacitor during the start-up transient.

In cases of very high output capacitive loads ($C_{LOAD}$ > 100 µF), all input/output capacitor values shall be modified as described in *Section 5.8.5: SCP and OCP operation with high capacitive load*.

The input ceramic capacitors should have a voltage rating in the range of 1.5 times the maximum input voltage and be located as close as possible to $V_{IN}$ pins.

## 5.3 Output capacitor ($V_{OUT}$ > 2.5 V)

The most important parameters for the output capacitor are the capacitance, the ESR and the voltage rating. The capacitance and the ESR affect the control loop stability, the output ripple voltage and transient response of the regulator.

The ripple due to the capacitance can be calculated with the following equation:

**Equation 3**

$$V_{RIPPLE(C)} = (0.125 \times \Delta I_{SW}) / (F_S \times C_{OUT})$$

where $F_S$ is the PWM switching frequency and $\Delta I_{SW}$ is the inductor peak-to-peak switching current, which can be calculated as:

**Equation 4**

$$\Delta I_{SW} = [(V_{IN} - V_{OUT}) / (F_S \times L)] \times D$$

where $D$ is the duty cycle.

The ripple due to the ESR is given by:

**Equation 5**

$$V_{RIPPLE}(ESR) = \Delta I_{SW} \times ESR$$

The equations above can be used to define the capacitor selection range, but final values should be verified by testing an evaluation circuit.

Lower ESR ceramic capacitors are usually recommended to reduce the output ripple voltage. Capacitors with higher voltage ratings have lower ESR values, resulting in lower output ripple voltage.

Also, the capacitor ESL value impacts the output ripple voltage, but ceramic capacitors usually have very low ESL, making ripple voltages due to the ESL negligible. In order to reduce ripple voltages due to the parasitic inductive effect, the output capacitor connection paths should be kept as short as possible.

The ST1S10 has been designed to perform best with ceramic capacitors. Under typical application conditions a minimum ceramic capacitor value of 22 µF is recommended on the output, but higher values are suitable considering that the control loop has been designed to work properly with a natural output LC frequency provided by a 3.3 µH inductor and 22 µF output capacitor. If the high capacitive load application circuit shown in *Figure 3* is used, a 47 µF (or 2 x 22 µF capacitors in parallel) could be needed as described in *Section 5.8.5: SCP and OCP operation with high capacitive load*.

The use of ceramic capacitors with voltage ratings in the range of 1.5 times the maximum output voltage is recommended.

## 5.4 Output capacitor (0.8 V < $V_{OUT}$ < 2.5 V)

For applications with lower output voltage levels ($V_{out}$ < 2.5 V) the output capacitance and inductor values should be selected in a way that improves the DC-DC control loop behavior. In this output condition two cases must be considered: $V_{IN}$ > 8 V and $V_{IN}$ < 8 V.

For $V_{IN}$ < 8 V the use of 2 x 22 µF capacitors in parallel to the output is recommended, as shown in *Figure 4.*

For $V_{IN}$ > 8 V, a 100 µF electrolytic capacitor with ESR < 0.1 Ω should be added in parallel to the 2 x 22 µF output capacitors as shown in *Figure 5.*

## 5.5 Output voltage selection

The output voltage can be adjusted from 0.8 V up to 85% of the input voltage level by connecting a resistor divider (see R1 and R2 in the typical application circuit) between the output and the $V_{FB}$ pin. A resistor divider with R2 in the range of 20 kΩ is a suitable compromise in terms of current consumption. Once the R2 value is selected, R1 can be calculated using the following equation:

**Equation 6**

$$R1 = R2 \times (V_{OUT} - V_{FB}) / V_{FB}$$

where $V_{FB}$ = 0.8 V (typ.).

Lower values are suitable as well, but will increase current consumption. Be aware that duty cycle must be kept below 85% at all application conditions, so that:

**Equation 7**

$$D = (V_{OUT} + V_F) / (V_{IN}-V_{SW}) < 0.85$$

where $V_F$ is the voltage drop across the internal NMOS, and $V_{SW}$ represents the voltage drop across the internal PDMOS.

Note that once the output current is fixed, higher $V_{OUT}$ levels increase the power dissipation of the device leading to an increase in the operating junction temperature. It is recommended to select a $V_{OUT}$ level which maintains the junction temperature below the

thermal shut-down protection threshold (150°C typ.) at the rated output current. The following equation can be used to calculate the junction temperature ($T_J$):

**Equation 8**

$$T_J = \{[V_{OUT} \times I_{OUT} \times R_{thJA} \times (1-\eta)] / \eta\} + T_{AMB}$$

where $R_{thJA}$ is the junction to ambient thermal resistance, $\eta$ is the efficiency at the rated $I_{OUT}$ current and $T_{AMB}$ is the ambient temperature.

To ensure safe operating conditions the application should be designed to keep $T_J < 140°C$.

## 5.6 Inductor ($V_{OUT} > 2.5$ V)

The inductor value fixes the ripple current flowing through output capacitor and switching peak current. The ripple current should be kept in the range of 20-40% of $I_{OUT\_MAX}$ (for example it is 0.6 - 1.2 A at $I_{OUT}$ = 3 A). The approximate inductor value can be obtained with the following equation:

**Equation 9**

$$L = [(V_{IN} - V_{OUT}) / \Delta I_{SW}] \times T_{ON}$$

where $T_{ON}$ is the ON time of the internal switch, given by:

$T_{ON} = D/F_S$

The inductor should be selected with saturation current ($I_{SAT}$) equal to or higher than the inductor peak current, which can be calculated with the following equation:

**Equation 10**

$$I_{PK} = I_O + (\Delta I_{SW}/2),\ I_{SAT} \geq I_{PK}$$

The inductor peak current must be designed so that it does not exceed the switching current limit.

## 5.7 Inductor (0.8 V < $V_{OUT}$ < 2.5 V)

For applications with lower output voltage levels ($V_{out} < 2.5$ V) the description in the previous section is still valid but it is recommended to keep the inductor values in a range from 1µH to 2.2 µH in order to improve the DC-DC control loop behavior, and increase the output capacitance depending on the $V_{IN}$ level as shown in *Figure 4* and *Figure 5.* In most application conditions a 2.2 µH inductor is the best compromise between DC-DC control loop behavior and output voltage ripple.

## 5.8 Function operation

### 5.8.1 Sync operation

The ST1S10 operates at a fixed frequency or can be synchronized to an external frequency with the SYNC pin. The ST1S10 switches at a frequency of 900 kHz when the SYNC pin is connected to ground, and can synchronize the switching frequency between 400 kHz to 1.2 MHz from an external clock applied to the SYNC pin. When the SYNC feature is not used,

this pin must be connected to ground with a path as short as possible to avoid any possible noise injected in the SYNC internal circuitry.

### 5.8.2 Inhibit function

The inhibit pin can be used to turn OFF the regulator when pulled down, thus drastically reducing the current consumption down to less than 6 µA. When the inhibit feature is not used, this pin must be tied to $V_{IN}$ to keep the regulator output ON at all times. To ensure proper operation, the signal source used to drive the inhibit pin must be able to swing above and below the specified thresholds listed in the electrical characteristics section under $V_{INH}$. Any slew rate can be used to drive the inhibit pin.

### 5.8.3 OCP (overcurrent protection)

The ST1S10 DC-DC converter is equipped with a switch overcurrent protection. In order to provide protection for the application and the internal power switches and bonding wires, the device goes into a shutdown state if the switch current limit is reached and is kept in this condition for the $T_{OFF}$ period ($T_{OFF(OCP)}$ = 135 µs typ.) and turns on again for the $T_{ON}$ period ($T_{ON(OCP)}$ = 22 µs typ.) under typical application conditions. This operation is repeated cycle by cycle. Normal operation is resumed when no overcurrent is detected.

### 5.8.4 SCP (short-circuit protection)

In order to protect the entire application and reduce the total power dissipation during an overload or an output short-circuit condition, the device is equipped with dynamic short-circuit protection which works by internally monitoring the $V_{FB}$ (feedback voltage).

In the event of an overload or output short-circuit, if the $V_{OUT}$ voltage is reduced causing the feedback voltage ($V_{FB}$) to drop below 0.3 V (typ.), the device goes into shutdown for the $T_{OFF}$ time ($T_{OFF(SCP)}$ = 288 µs typ.) and turns on again for the $T_{ON}$ period ($T_{ON(SCP)}$ = 130 µs typ.). This operation is repeated cycle by cycle, and normal operation is resumed when no overload is detected ($V_{FB}$ > 0.3 V typ.) for the full $T_{ON}$ period.

This dynamic operation can greatly reduce the power dissipation in overload conditions, while still ensuring excellent power-on startup in most conditions.

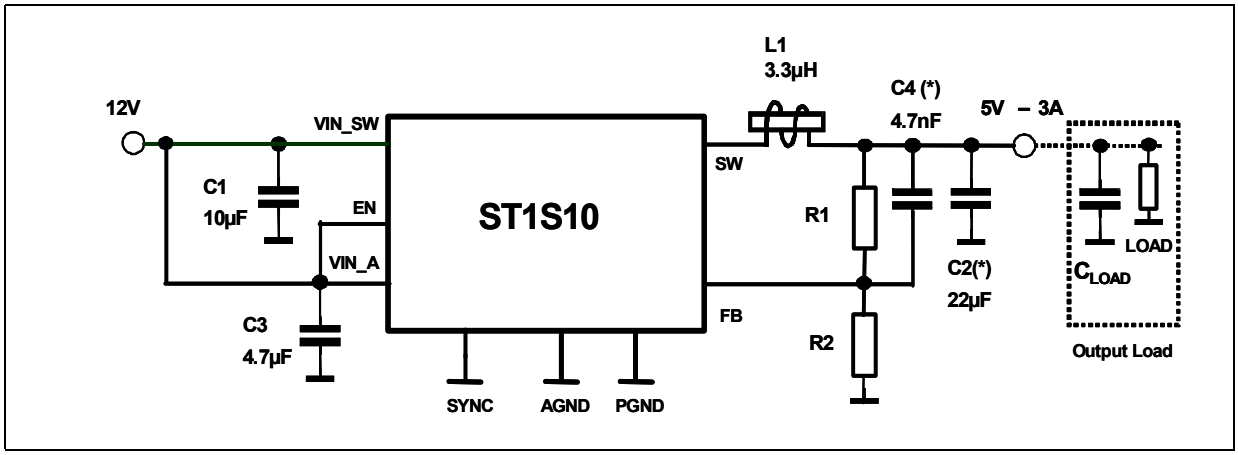
### 5.8.5 SCP and OCP operation with high capacitive load

Thanks to the OCP and SCP circuit, ST1S10 is strongly protected against damage from short-circuit and overload.

However, a highly capacitive load on the output may cause difficulties during start-up. This can be resolved by using the modified application circuit shown in *Figure 3*, in which a minimum of 10 µF for C1 and a 4.7 µF ceramic capacitor for C3 are used. Moreover, for $C_{LOAD}$ > 100 µF, it is necessary to add the C4 capacitor in parallel to the upper voltage divider resistor (R1) as shown in *Figure 3.* The recommended value for C4 is 4.7 nF.

Note that C4 may impact the control loop response and should be added only when a capacitive load higher than 100 µF is continuously present. If the high capacitive load is variable or not present at all times, in addition to C4 an increase in the output ceramic capacitor C2 from 22 µF to 47 µF (or 2 x 22 µF capacitors in parallel) is recommended. Also in this case it is suggested to further increase the input capacitors to a minimum of 10 µF for C1 and a 4.7 µF ceramic capacitor for C3 as shown in *Figure 3.*

Figure 3. Application schematic for heavy capacitive load




(*) see OCP and SCP descriptions for C2 and C4 selection.

Figure 4. Application schematic for low output voltage ($V_{OUT}$ < 2.5 V) and 2.5 V < $V_{IN}$ < 8 V

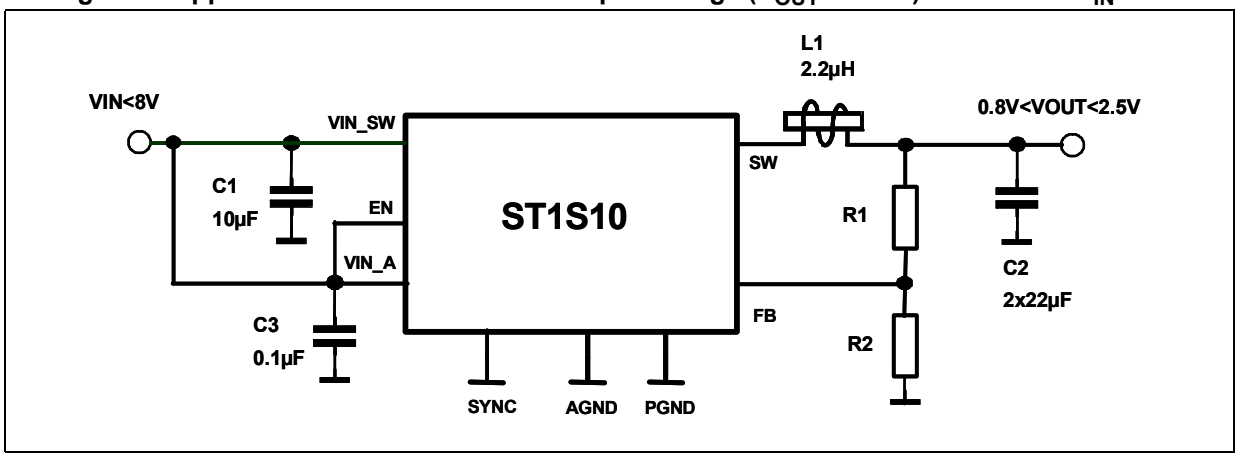
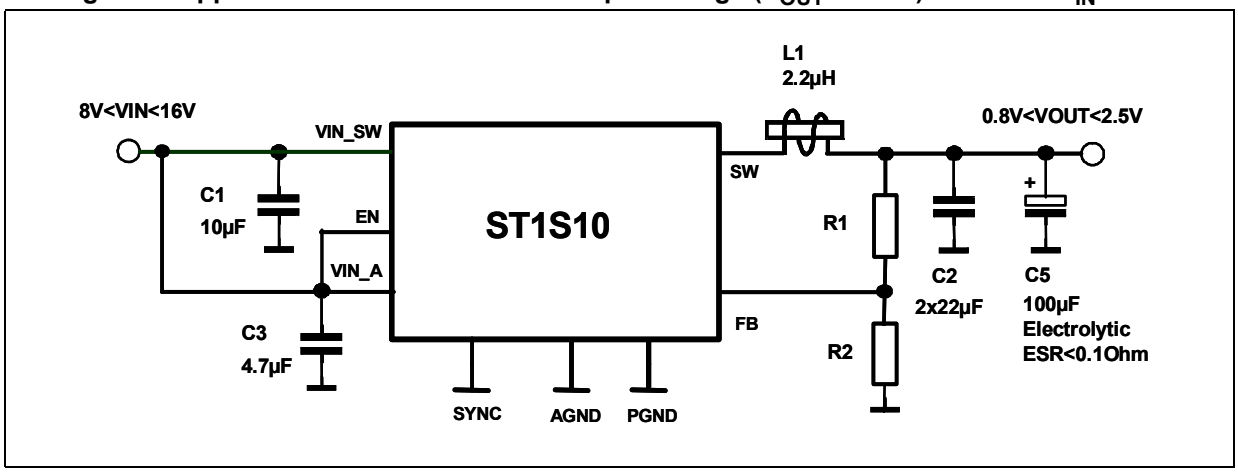



Figure 5. Application schematic for low output voltage ($V_{OUT}$ < 2.5 V) and 8 V < $V_{IN}$ < 16 V



# 6 Layout considerations

The layout is an important step in design for all switching power supplies.

High speed operation (900 kHz) of the ST1S10 device demands careful attention to PCB layout. Care must be taken in board layout to get device performance, otherwise the regulator could show poor line and load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node for power ground and a different one for control ground (AGND) to minimize the effects of ground noise. Connect these ground nodes together underneath the device and make sure that small signal components returning to the AGND pin and do not share the high current path of $C_{IN}$ and $C_{OUT}$.

The feedback voltage sense line ($V_{FB}$) should be connected right to the output capacitor and routed away from noisy components and traces (e.g.: SW line). Its trace should be minimized and shielded by a guard-ring connected to the ground.

**Figure 6. PCB layout suggestion - top**

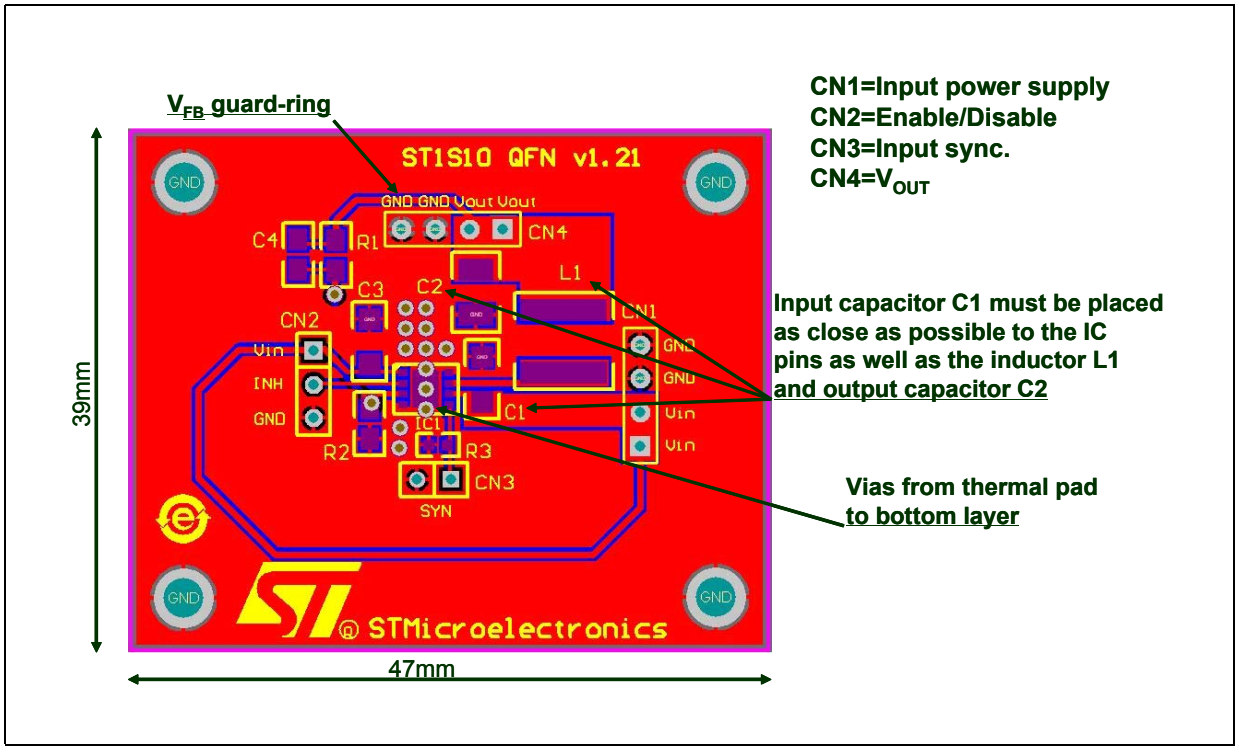
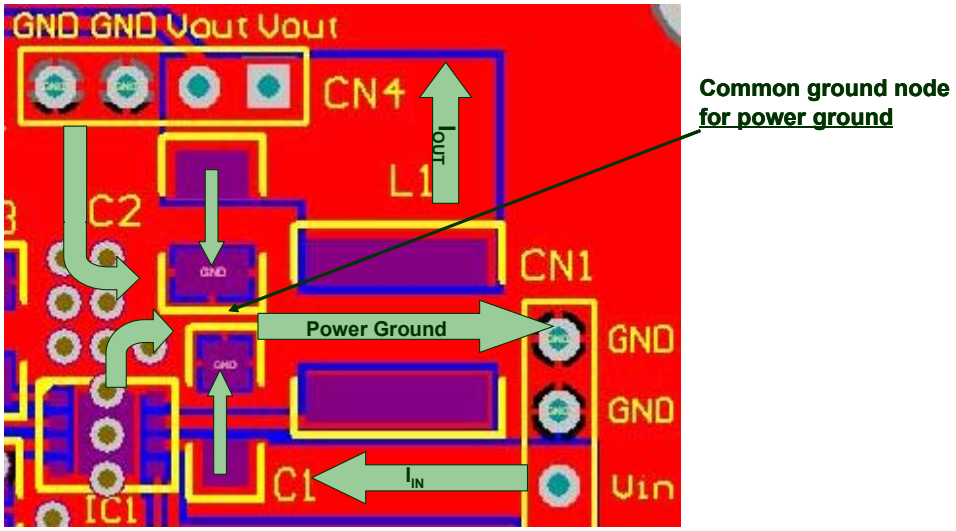


Figure 7. PCB layout suggestion - bottom

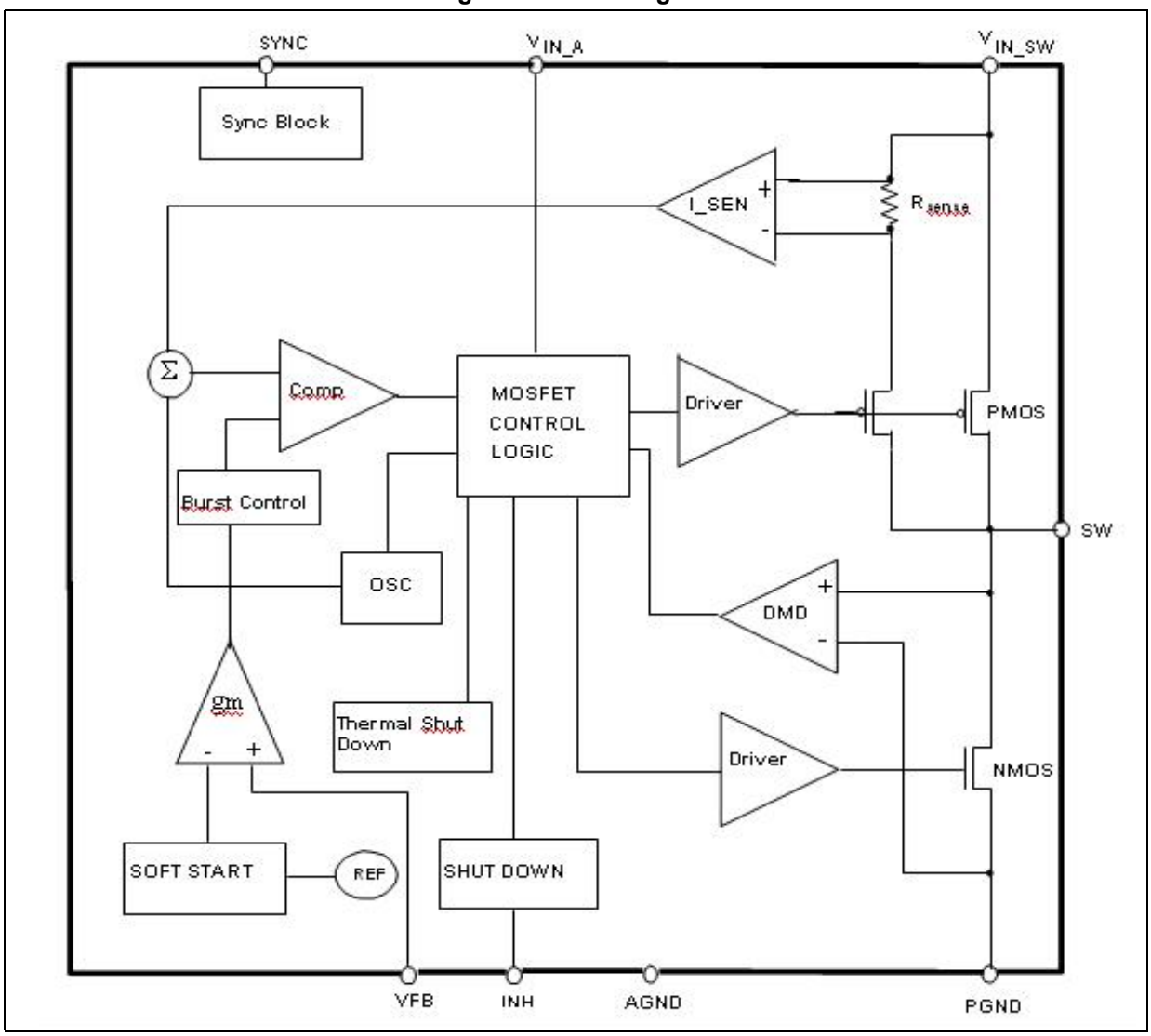



## Thermal considerations

The lead frame die pad, of the ST1S10, is exposed at the bottom of the package and must be soldered directly to a properly designed thermal pad on the PCB, the addition of thermal vias from the thermal pad to an internal ground plane will help increase power dissipation.

# 7 Diagram

**Figure 8. Block diagram**



# 8 Typical performance characteristics

Unless otherwise specified, refer to the typical application circuit under the following conditions: $T_J$ = 25 °C, $V_{IN}$ = $V_{IN-SW}$ = $V_{IN-A}$ = $V_{INH}$ = 12 V, $V_{SYNC}$ = GND, $V_{OUT}$ = 5 V, $I_{OUT}$ = 10 mA, $C_{IN}$ = 4.7 µF + 0.1 µF, $C_{OUT}$ = 22 µF, L1 = 3.3 µH.

**Figure 9. Voltage feedback vs. temperature**

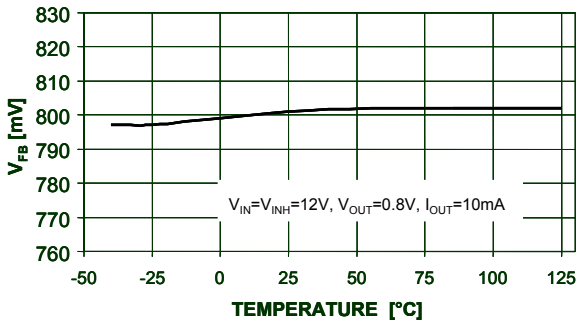



**Figure 10. Oscillator frequency vs. temperature**

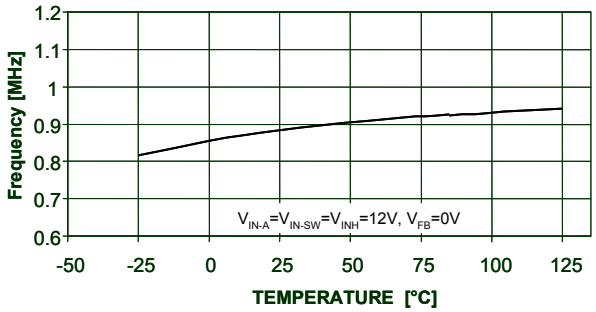



**Figure 11. Max. duty cycle vs. temperature**

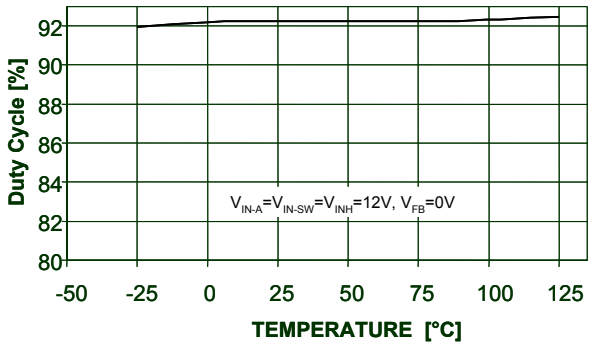



**Figure 12. Inhibit threshold vs. temperature**

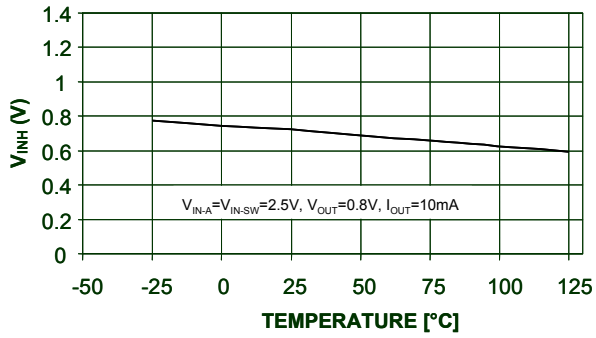


**Figure 13. Reference line regulation vs. temperature**

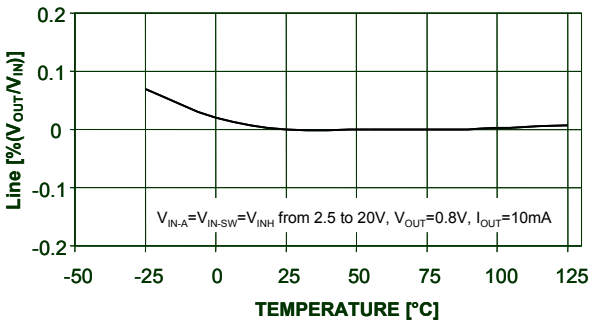



**Figure 14. Reference load regulation vs. temperature**

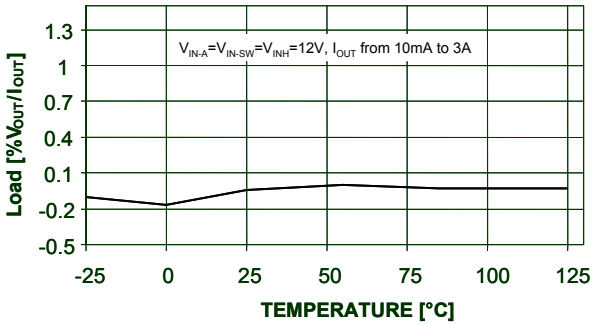



**Figure 15. ON mode quiescent current vs. temperature**

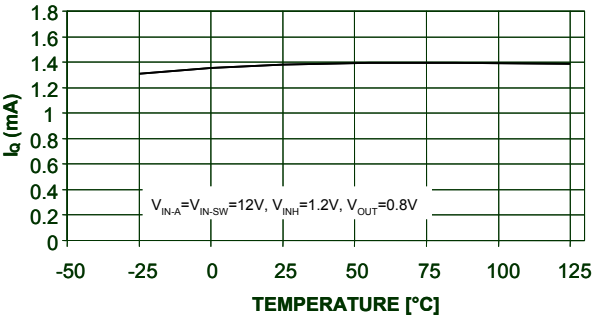



**Figure 16. Shutdown mode quiescent current vs. temperature**

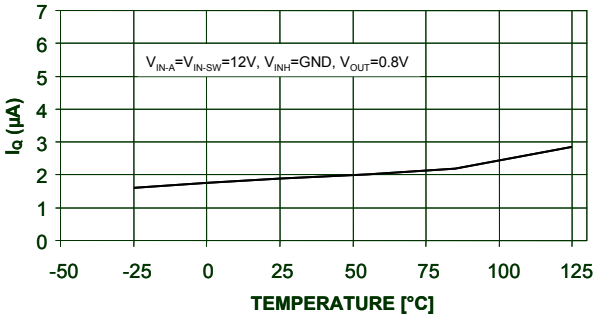



**Figure 17. PMOS ON resistance vs. temperature**

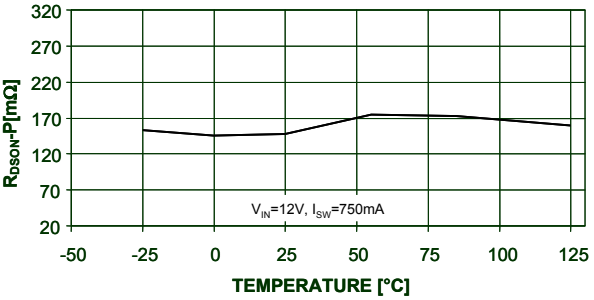



**Figure 18. NMOS ON resistance vs. temperature**

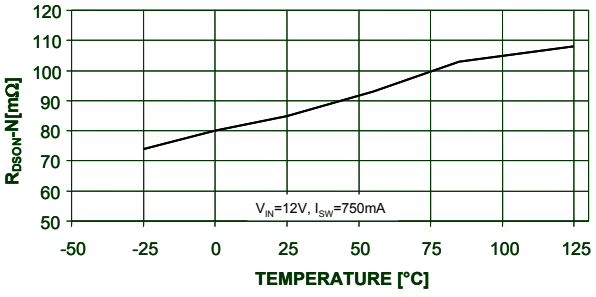


Figure 19. Efficiency vs. temperature

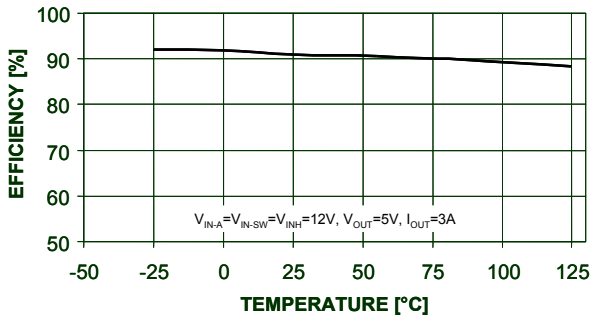



Figure 20. Efficiency vs. output current at $V_{out}$ = 5 V

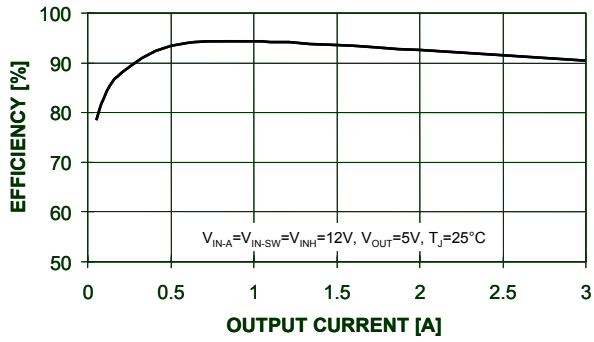



Figure 21. Efficiency vs. output current at $V_{out}$ = 3.3 V

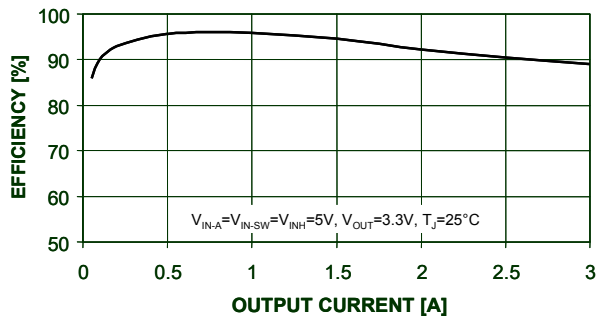
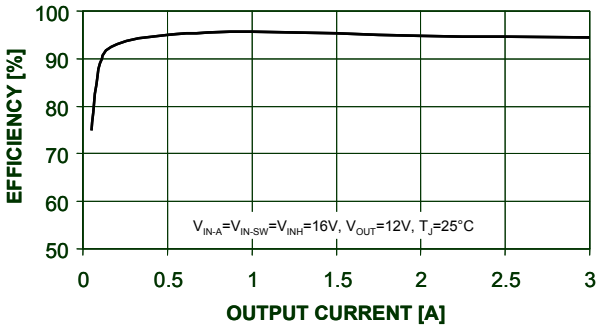



Figure 22. Efficiency vs. output current at $V_{out}$ = 12 V



# 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 9.1 Power SO-8 package information

**Figure 23. Power SO-8 (exposed pad) package outline**

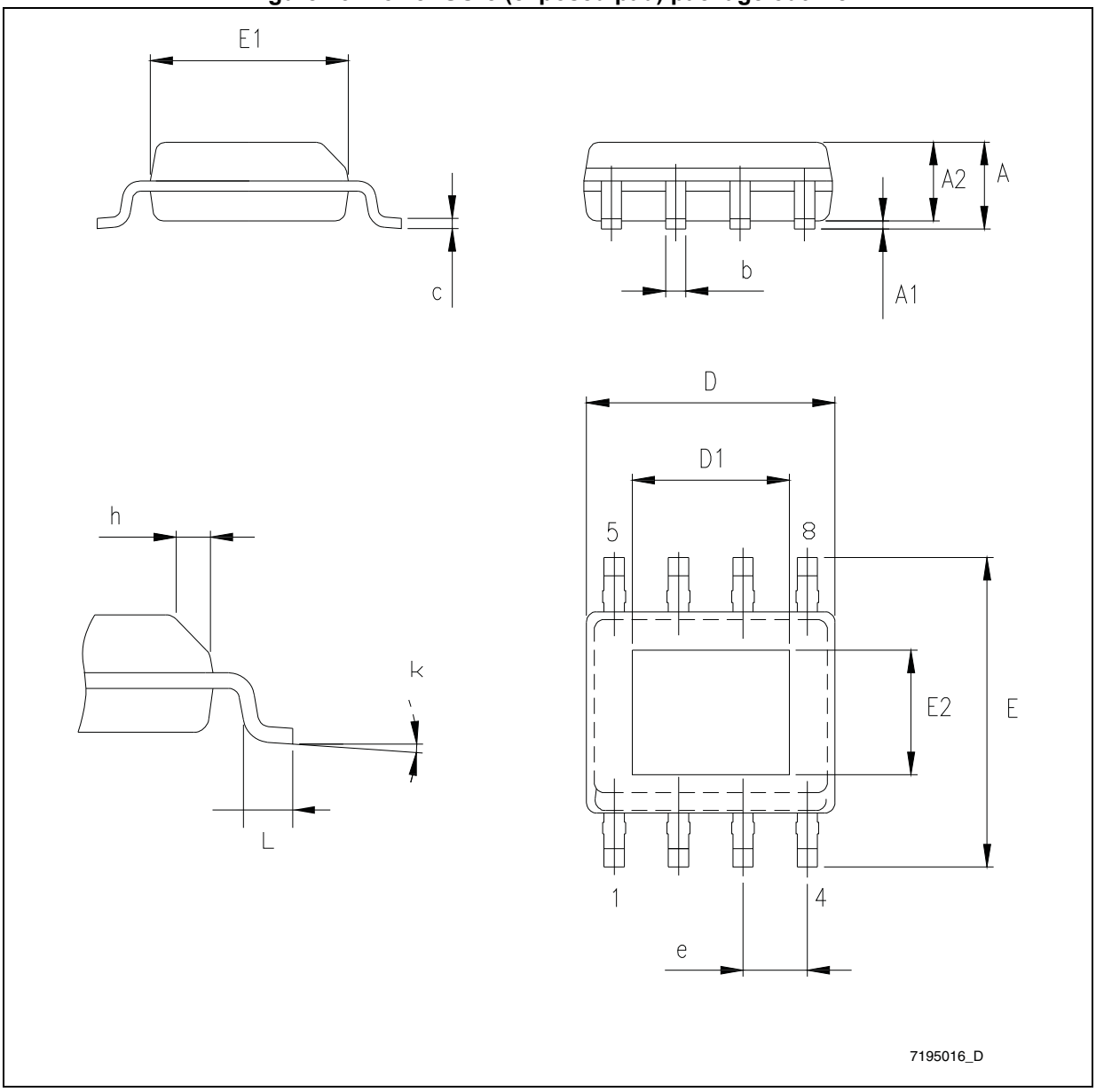


Table 7. Power SO-8 (exposed pad) package mechanical data

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.70 |
| A1 | 0.00 | | 0.15 |
| A2 | 1.25 | | |
| b | 0.31 | | 0.51 |
| c | 0.17 | | 0.25 |
| D | 4.80 | 4.90 | 5.00 |
| D1 | ACCORDING TO PAD SIZE | | |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| E2 | ACCORDING TO PAD SIZE | | |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| K | 0 | | 8 |
| ccc | | | 0.10 |

*Note: Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).*

*Dimension “E1” does not include interlead flash or protrusions.*

*Interlead flash or protrusions shall not exceed 0.25mm per side.*

*The size of exposed pad is variable depending of leadframe design pad size.*

*End user should verify “D1” and “E2” dimensions for each device application.*

**Figure 24. Power SO-8 (exposed pad) recommended footprint**

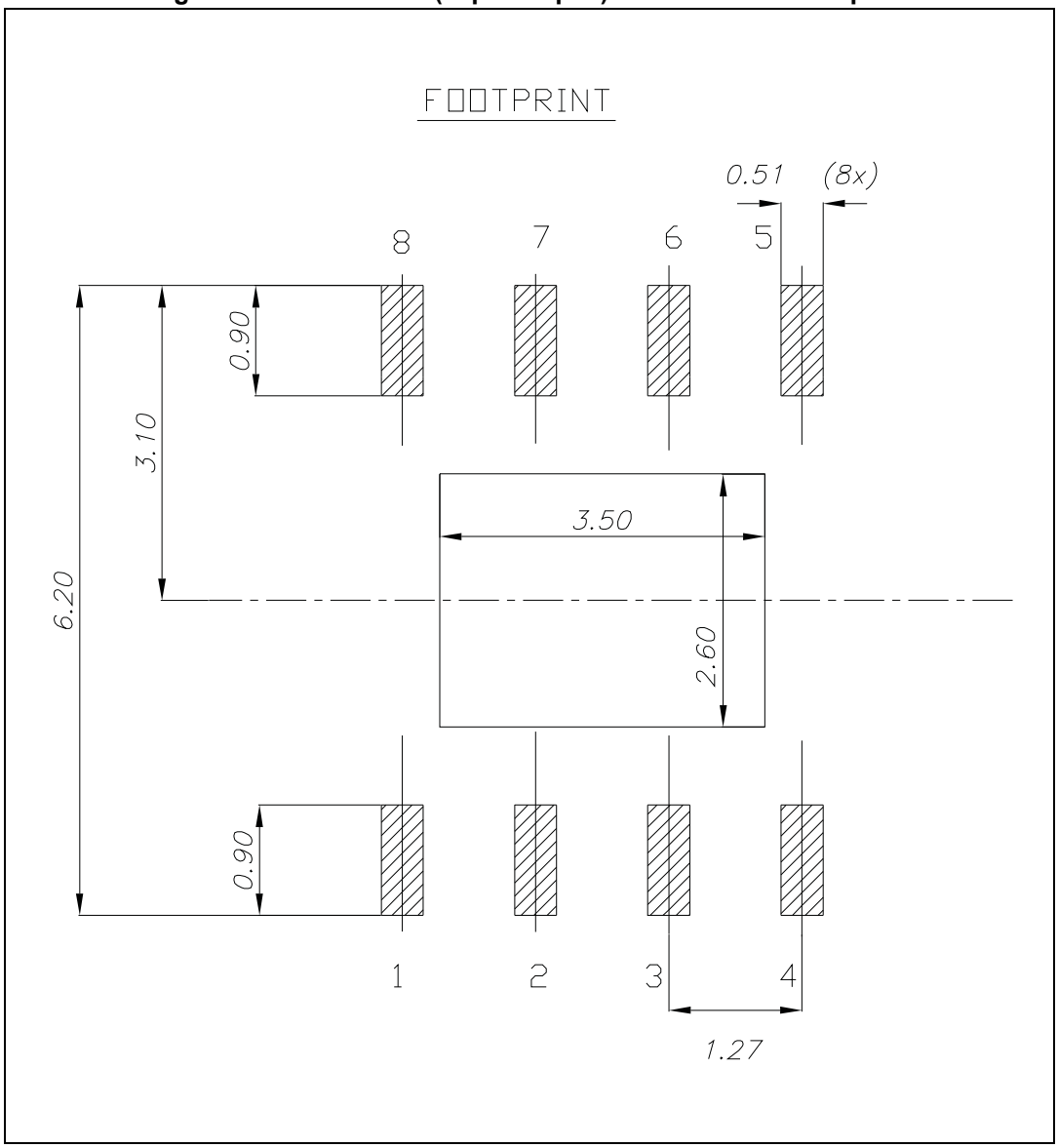


Figure 25. Power SO-8 (exposed pad) tape and reel dimensions

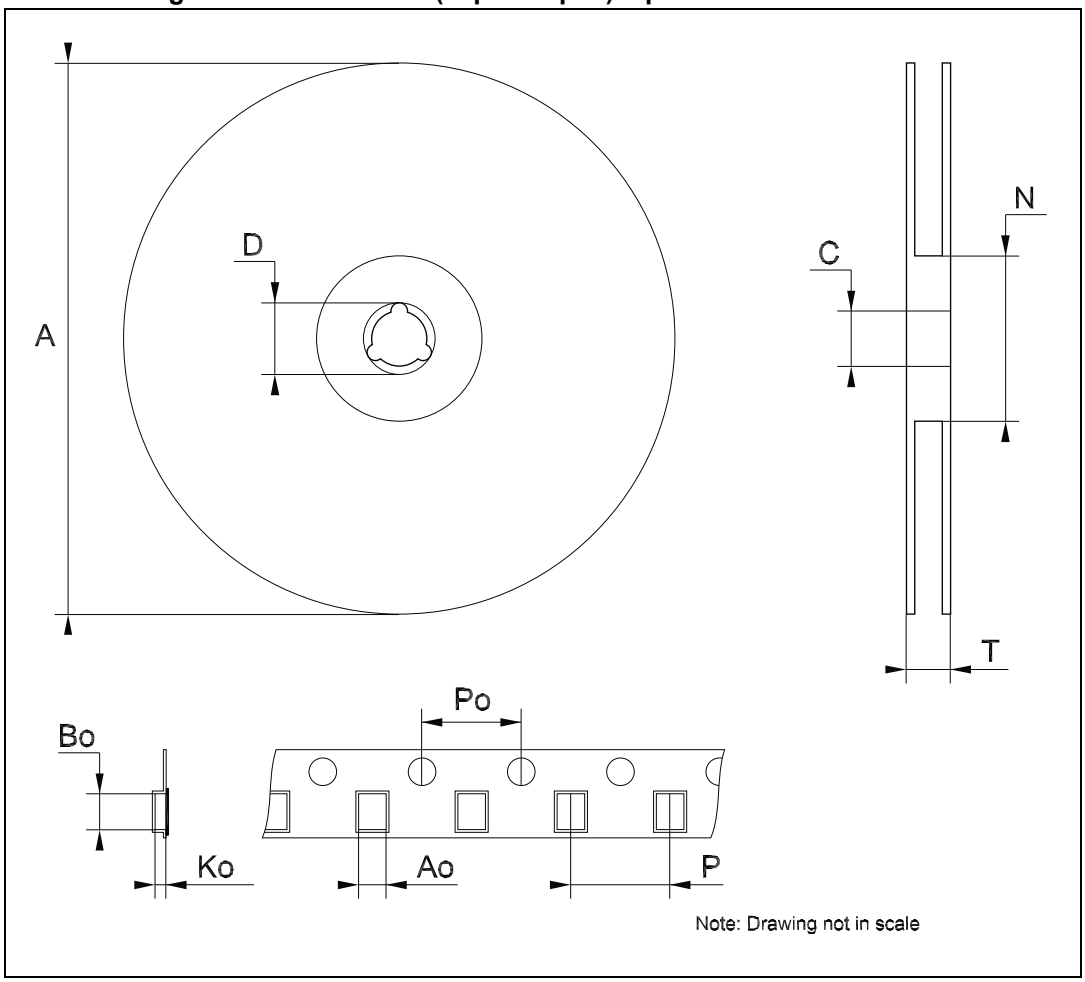



Table 8. Power SO-8 (exposed pad) tape and reel mechanical data

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 8.1 | | 8.5 |
| Bo | 5.5 | | 5.9 |
| Ko | 2.1 | | 2.3 |
| Po | 3.9 | | 4.1 |
| P | 7.9 | | 8.1 |

## 9.2 DFN8 (4 x 4) package information

**Figure 26. DFN8 (4 x 4) package outline**

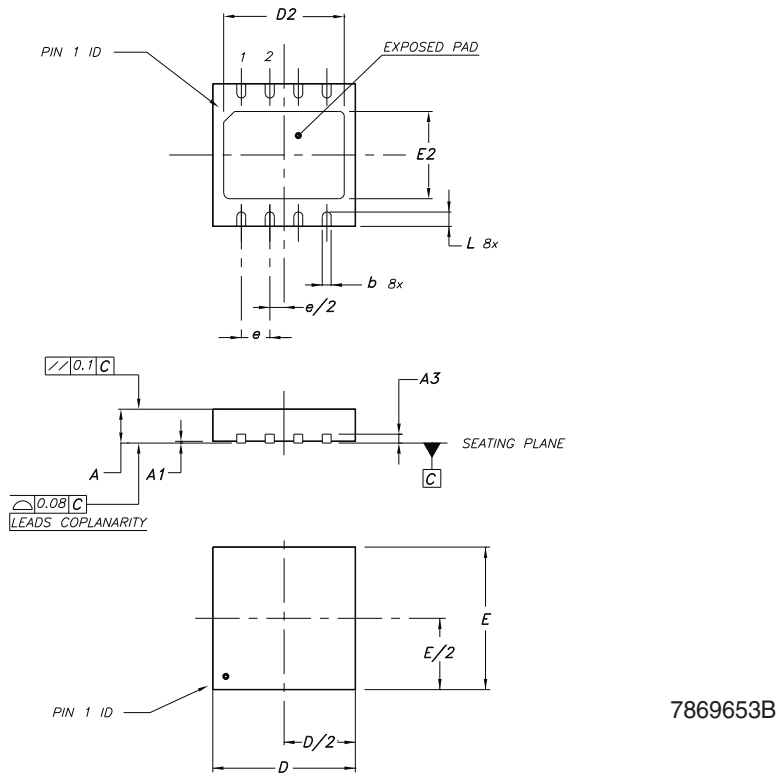



**Table 9. DFN8 (4 x 4) package mechanical data**

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.20 | |
| b | 0.23 | 0.30 | 0.38 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.82 | 3.00 | 3.23 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.05 | 2.20 | 2.30 |
| e | | 0.80 | |
| L | 0.40 | 0.50 | 0.60 |

Figure 27. DFN8 (4 x 4) tape and reel dimensions

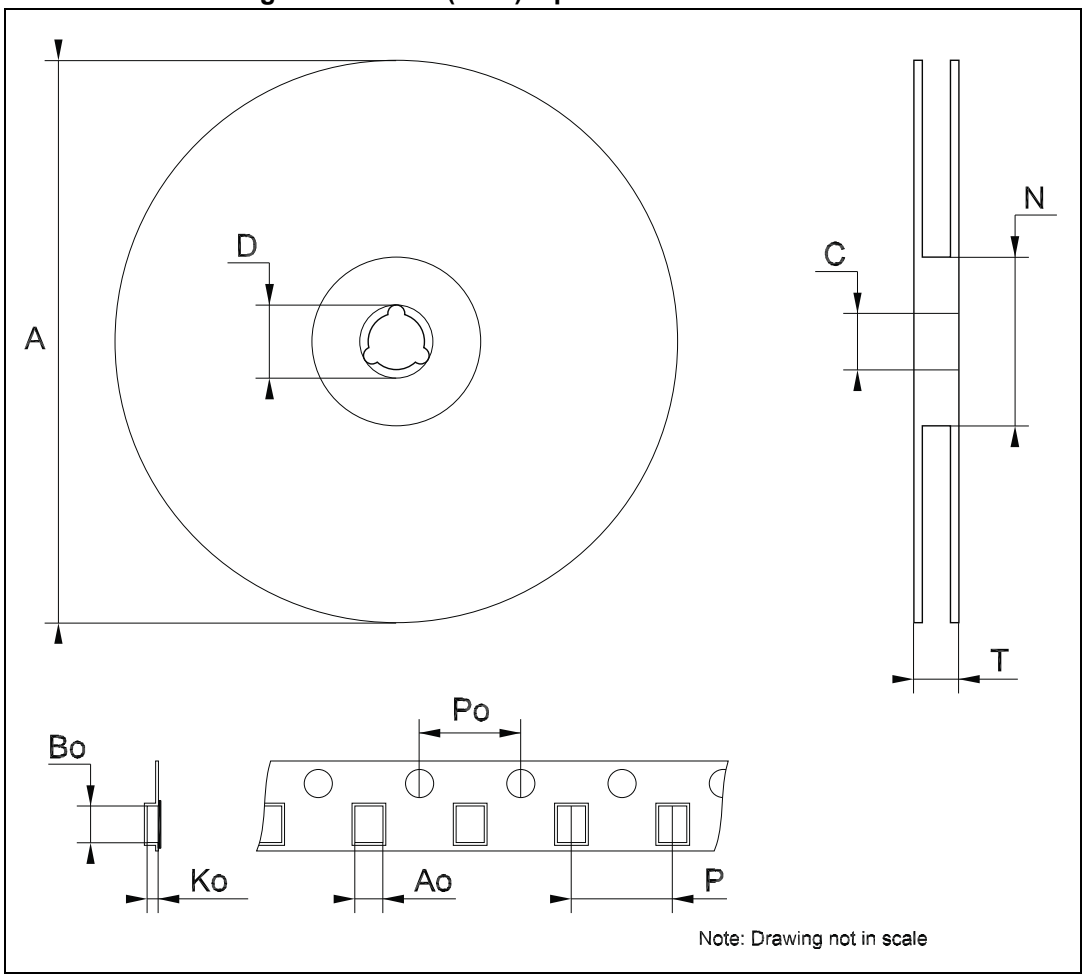



Table 10. DFN8 (4 x 4) tape and reel mechanical data

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 99 | | 101 |
| T | | | 14.4 |
| Ao | | 4.35 | |
| Bo | | 4.35 | |
| Ko | | 1.1 | |
| Po | | 4 | |
| P | | 8 | |

# 10 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 28-Aug-2007 | 1 | Initial release. |
| 24-Sep-2007 | 2 | Add $R_{thJC}$ on *Table 4.* |
| 25-Oct-2007 | 3 | Added new paragraph *6: Layout considerations*. |
| 16-Mar-2010 | 4 | Updated PowerSO-8 package mechanical data. |
| 31-May-2012 | 5 | Updated SO-8 (epad) and DFN8 (4x4) mechanical data.<br>Changed temperature min from 25 °C to 40 °C in *Table 4*, and in *Section 4*. |
| 27-Mar-2015 | 6 | Added *Table 5: ESD protection on page 8*.<br>Added and updated cross-references throughout document.<br>Updated titles of *Figure 6 on page 17* and *Figure 7 on page 18*.<br>Updated *Section 9: Package information on page 23* (updated/added titles, headers, reformatted section).<br>Minor modifications throughout document. |